UNITED STATES PATENT AND TRADEMARK OFFICE

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EXAMINER
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ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/22/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

	Application No.	Applicant(s)
Office Action Summary	10/662,093	GILBERT ET AL.
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _06 December 2006_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1,3-31 and 33_ is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1,3-31 and 33_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set

forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this

application is eligible for continued examination under 37 CFR 1.114, and the fee set

forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action

has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on

December 6, 2006, has been entered.

2.   In response to the Advisory action mailed on October 16, 2006, claims 2 and 32

have been canceled. Claims 1, 3-5, 11, 14, 18, 21, 24-28, and 31 have been amended.

As a result, claims 1, 3-31, and 33 remain pending.

Response to Arguments

3.   Applicant's arguments filed December 6, 2006, have been fully considered but

they are not persuasive.

    a.   Applicants argue on pages 8-9 of the remarks that the evidence provided

    is sufficient to overcome the rejection for lack of enablement under 35 USC 112

    first paragraph. Applicants also argue that "when claims 11, 14, 18, 21, 24, and

    28 use the term "inner relationship", it implies that the first cache is closer to the

    processor than the second cache."

        i.   Examiner would like to make it clear that the issue here is not

        whether L1 cache is closer to the processor than L2 cache since that's

well known in the art and by definition, an L1 cache is closer to the

processor than an L2 cache. Rather, simply because the specification

mentions the words "inner" and "outer" in describing L1 and L2 caches

does not make the disclosure enabling for the limitation "inner relationship"

recited in independent claims 11, 14, 18, 21, 24, and 28. Furthermore,

Examiner would like to mention that in the specification an "inner cache" is

being referred to as an L1 cache and "outer cache" as an L2 cache. In this

case, should Examiner assume that "inner relationship" is being referred

to as "L1 relationship"? As such, the evidence provided by Applicant is still

not sufficient to overcome the rejection for lack of enablement under 35

USC 112, first paragraph and Applicants simply mention that one of

ordinary skill in the would have known that an L1 cache is closer to the

processor than an L2 cache as evidence supporting his contention that the

limitations "inner relationship" and "outer relationship" are enabled. Such

contention has no bearing whatsoever on the facts stated in the Office

action making those limitations not enabling.

ii.   Additionally, Once the examiner has established a prima facie case

of lack of enablement, the burden falls on the Applicant to present

persuasive arguments, supported by suitable proofs where necessary,

that one skilled in the art would have been able to make and use the

claimed invention using the disclosure as a guide. *In re Brandstadter, 484*

F.2d 1395, 179 USPQ 286 (CCPA 1973). Evidence to supplement a

specification which on its face appears deficient under 35 USC 112 must

establish that the information which must be read into the specification to

make it complete would have been known to those of ordinary skill in the

art.

Therefore, the Examiner strictly maintains claims 11, 14, 18, 21, 24,

and 28 as not being enabled by the disclosure.

b.   Applicants argue on page 10 of the remarks that the combination of

Arimilli_1 and the WO reference does not teach or suggest "a cache containing a

cache line with a first cache coherency state when accessed from said first

interface and a second cache coherency state when accessed from said second

interface".

Examiner respectfully disagrees with such assertion. Fig. 1 of WO clearly

shows a cache (CS) accessible by a plurality of processors (EPs) through a first

interface (BS1) on one side and accessible by additional cache memories, main

memory (MEM), or all types of I/O through a second interface (BS2). If a line was

recently cached from main memory (MEM) through BS2, said cache line is in the

exclusive state, and if one of the processors (EPs) wants to read the cache line,

and performs some operation that require changing the state of the cache to

modified, another associated processor (EP) trying to read the same cache line

through interface BS1 would find it in a modified state; See Fig. 1, p. 6 et seq.

In addition to that, WO clearly discloses that "the state of a cache block may be altered by a particular assigned processor (EP) via a read and write procedure (through interface BS1); the state may also be altered by an internal system query, also known as snooping; it may also be altered by external logic units (through interface BS2), e.g., another individual processor or a second level cache memory, i.e., through external snooping; p. 2, par. 5 to p. 3, par. 1 et seq.", as shown in the processor system of Fig. 1 which is "constructed hierarchically with lower hierarchy stages situated in the direction of first bus BS1 and higher hierarchy stages situated in the direction of second bus BS2; p. 6, par. 4 et seq.". Furthermore, WO discloses "requests can be made between the additional cache memories CS and the individual processors EP (through interface BS1 processors EP guarantee access of a cache line with a first coherency state), and requests between additional cache memories CS and the main memory (through cache memory bus BS2 guarantee accessing a cache line with a second coherency state); p.7, par. 4.

Still further WO discloses "if an SLC has requested an entry of the TLC using the command RDE or RDM and then modified it, it has to ensure that the modified entry is written back in the TLC using the WR command...after the modification of the requested entry (through BS2, See Fig. 1) the requesting SLC may maintain the entry in modified form and identify is as such. It may also write back the entry and, and as a result of writing back (to main memory MEM or TLC through BS2) downgrade the state of the entry and only still put it in the state

E...If the cache memory block is requested by an individual processor EP

(through BS1, See Fig. 1) situated in a lower hierarchy, the TLC knows that the

cache memory block has been changed...".; See p. 11 et seq..

c.   Applicants argue on page 12 of the remarks that the combination of

Arimilli_1 and Arimilli_2 does not teach or suggest the limitation of "**TWO** cache

coherency states associated with one cache line".

In response to applicant's argument that the references fail to show certain

features of applicant's invention, it is noted that the features upon which applicant

relies (i.e., "**TWO** cache coherency states associated with one cache line") are

not recited in the rejected claim(s). Although the claims are interpreted in light of

the specification, limitations from the specification are not read into the claims.

See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

d.   Applicants further argue on page 12 that Arimilli_2 does not disclose the

limitation of "**TWO** cache coherency states associated with one cache line".

Examiner would like to point out that Arimilli_1 and the WO reference are

relied upon for rejecting the teachings of claim 1 and the features argued

by Applicants are not claimed.

e.   Applicants still argue on page 12 of the remarks that the combination of

Arimilli_1, Arimilli_2 and the WO reference does not teach "the first cache

coherency state has higher privilege than the second cache coherency state

when the second interface is coupled to a processor", recited in claim 1.

Examiner respectfully disagrees and would like to point out that Arimilli_2

clearly discloses "protecting the ownership of a shared cache line by an

agent that wins ownership of a shared cache line during arbitration; once

the coherency protocol has granted ownership of a shared cache line to a

first agent for purposes of modification, the coherency protocol cannot

permit another agent to gain ownership of the same cache line until the

first agent has completed modification of the cache line and all other

agents have agreed to invalidate their cached copies of the line; par. 10."

f.   Applicants argue on page 13 of the remarks that there is no showing by

the cited portions of the WO reference of transitions from a single MESI

coherency state (e.g., M or E) to a joint coherency state (e.g., MI) as recited by

the claimed invention.

Examiner respectfully disagrees. The WO reference clearly shows single

MESI TLC state (e.g., I, S, E, M) and single MESI SLC state (e.g., I, S, E,

M) transitioning to joint coherency state (e.g., SI ES, EM, MI, MI, MS...).

g.   In view of the foregoing discussion, the rejection of claims 1, 3-31, and 33

is strictly maintained and reiterated below.

Claim Rejections - 35 USC § 103.

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1, 3-10, and 31,33 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Arimilli (6,629,268) in view of WO 00/52582 and further in view of

Arimilli (2002/0129211).

As per claim 1, Arimilli (6,629,268) discloses an apparatus, comprising: a first

interface [Fig.2; Bus Interface Unit 35]; a second interface not directly coupled to said

first interface [Fig.2; Interface 18]; and a cache accessible from said first interface and

said second interface [Fig.2; L2 cache, Bus Interface 35, Interface 19; col.8, lines 6-33].

However, Armilli (268) does not specifically teach a cache containing a cache

line with a first cache coherency state when accessed from said first interface and a

second cache coherency state when accessed from said second interface as required.

WO 00/52582 discloses a cache containing a cache line with a first cache

coherency state when accessed from said first interface and a second cache coherency

state when accessed from said second interface [Fig. 1; page 11, ll 16-32; page 12, ll

21-27] to increase the performance capability of processor systems while ensuring that

the cache memory block is not read unnecessarily (page 1, ll 1-5; page 11, ll 18-23).

Since the technology for implementing a cache memory system with a cache

containing a cache line with a first cache coherency state when accessed from said first

interface and a second cache coherency state when accessed from said second

interface was well known as evidenced by WO 00/52582, an artisan would have been

motivated to implement this feature in the system of Arimilli (268) in order to increase

the performance capability of processor systems while ensuring that the cache memory

block is not read unnecessarily. Thus, it would have been obvious to one of ordinary

skill in the art at the time of invention by Applicant to modify the system of Arimilli (268)

to include a cache containing a cache line with a first cache coherency state when

accessed from said first interface and a second cache coherency state when accessed

from said second interface since this would have increased the performance capability

of processor systems while ensuring that the cache memory block is not read

unnecessarily (page 1, ll 1-5; page 11, ll 18-23) as taught by WO 00/52582.

Arimilli (268) and WO disclose the claimed invention as discussed above in the

previous paragraphs. However, Arimilli (268) and WO do not specifically teach the first

cache coherency state has higher privilege than said second cache coherency state

when said second interface is coupled to a processor as required by the claims.

Arimilli (2002/0129211) discloses the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor [par. 10] to resolve conflicts between requests to modify a cache line (par. 2).

Since the technology for implementing a cache system with the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor was well known as evidenced by Arimilli (211), an artisan would have been motivated to implement this feature in the system of Arimilli (268) and WO in order to resolve conflicts between requests to modify a cache line. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Armilli (268) and WO to include the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor because this would have resolved conflicts between requests to modify a cache line (par. 2).

As per claim 31, the rationale in the rejection of claim 1 is herein incorporated. Arimilli (268) further discloses a bus bridge to a third interface [Fig.1]; and an input-output device coupled to a third interface [Fig.3].

As per claim 3, Arimilli (211) discloses a second cache coherency state is to reduce snoop transactions on said second interface [par. 5].

As per claim 4, Arimilli (211) discloses said first cache coherency state is exclusive and said second cache coherency state is shared [pars. 6, 24 and 36].

As per claim 5, Arimilli (211) discloses first cache coherency state is modified and said second cache coherency state is shared [par. 8].

As per claim 6, Arimilli (211) discloses second cache coherency state supports speculative invalidation [par. 6]. .

As per claim 7, Arimilli (211) discloses first cache coherency state is modified and said second cache coherency state is invalid [par. 7].

As per claim 8, Arimilli (211) discloses first cache coherency state is exclusive and said second cache coherency state is invalid [pars. 6 and 36].

As per claim 9, Arimilli (211) discloses the first cache coherency state is shared and said second cache coherency state is invalid [par. 7].

As per claim 10, Arimilli (211) discloses the second cache coherency state further supports explicit invalidation [pars. 7 and 10].

As per claim 33, the rationale in the rejection of claim 3 is herein incorporated.

6.   Claims 11-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Arimilli (2002/0129211) in view of WO 00/52582.

As per claim 11, Armilli (211) discloses a method, comprising: associating a first

cache coherency state with a first cache line in a first cache [par. 10]; associating a

second cache coherency state with a second cache line in a second cache in an inner

relationship to said first cache [pars. 24 and 29];

However, Arimilli (211) does not specifically teach transitioning a first cache

coherency state to a joint cache coherency state including a first cache coherency state

for outer interfaces and a third cache coherency state for inner interfaces; and

transitioning a second cache coherency state to a third cache coherency state as

required by the claim.

WO 00/52582 discloses transitioning a first cache coherency state to a joint

cache coherency state including a first cache coherency state for outer interfaces and a

third cache coherency state for inner interfaces [Fig. 3; page 7, ll 27 to page 8, ll 13;

page 15; ll 1-19]; and transitioning a second cache coherency state to a third cache

coherency state [Fig .3; page 15, ll 15-19] to allow the cache to have a deeper

knowledge about the state situation within the processor system, which allows it to relay

and/or capture requests directed to the individual processors (page 15, ll 22-25).

Since the technology for implementing a cache system with transitioning a first

cache coherency state to a joint cache coherency state including a first cache

coherency state for outer interfaces and a third cache coherency state for inner

interfaces was well known as evidenced by WO 00/52582, an artisan would have been

motivated to implement this feature in the system Arimilli (211) since this would have

allowed the cache to have a deeper knowledge about the state situation within the

processor system, which allows it to relay and/or capture requests directed to the

individual processors. Thus, it would have been obvious to one of ordinary skill in the art

at the time of invention by Applicant to modify the system of Arimilli (211) to include

transitioning a first cache coherency state to a joint cache coherency state including a

first cache coherency state for outer interfaces and a third cache coherency state for

inner interfaces in order to the cache to have a deeper knowledge about the state

situation within the processor system, which allows it to relay and/or capture requests

directed to the individual processors (page 15, ll 22-25) as taught by WO 00/52582.

As per claim 12, WO 00/52582 discloses a first cache coherency state is

exclusive, a second cache coherency state is invalid, and a third cache coherency state

is shared [Fig. 3].

As per claim 13, WO 00/52582 discloses a first cache coherency state is

modified, said second cache coherency state is modified, and said third cache

coherency state is invalid [Fig. 3].

As per claim 14, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 15, Arimilli (211) discloses the first cache coherency state is modified [par. 36].

As per claim 16, Arimilli (211) discloses the first cache coherency state is exclusive [par. 36].

As per claim 17, Arimilli (211) discloses the first cache coherency state is shared [par. 37].

As per claim 18, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 19, WO 00/52582 discloses the first cache coherency state is invalid and the joint cache coherency state is exclusive-shared [Fig. 3].

As per claim 20, WO 00/52582 discloses the first cache coherency state is modified-invalid and the joint cache coherency state is modified-shared [Fig. 3].

As per claim 21, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 22, the rationale in the rejection of claim 12 is herein incorporated.

As per claim 23, the rationale in the rejection of claim 13 is herein incorporated.

As per claim 24, the rationale in the rejection of claim 14 is herein incorporated.

As per claim 25, the rationale in the rejection of claim 15 is herein incorporated.

As per claim 26, the rationale in the rejection of claim 16 is herein incorporated.

As per claim 27, the rationale in the rejection of claim 17 is herein incorporated.

As per claim 28, the rationale in the rejection of claim 18 is herein incorporated.

As per claim 29, the rationale in the rejection of claim 19 is herein incorporated.

As per claim 30, the rationale in the rejection of claim 20 is herein incorporated.

Conclusion

7.   When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

8.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sough Hyung can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

December 20, 2006

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SUPERVISORY PATENT EXAMINER
12/21/06

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